

ABSTRACT OF THE DISCLOSURE

1 A synchronous memory device and methods of operation and
2 controlling such a device. The synchronous memory device includes
3 clock receiver circuitry to receive an external clock signal and input
4 receiver circuitry to sample a first operation code synchronously with
5 respect to a transition of the external clock signal. The synchronous
6 memory device also includes a programmable register to store a binary
7 value, wherein the memory device stores the binary value in the
8 programmable register in response to the first operation code.

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